Short Form Specification

mifare® & I•CODE

CL RC632

Multiple Protocol Contactless Reader IC

Short Form Specification

Revision 3.2

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Philips Semiconductors

PHILIPS

CONTENTS

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1 INTRODUCTION

1.1 Scope

The CL RC632 is member of a new family of highly integrated reader ICs for contactless communication at 13.56 MHz. This reader IC family utilises an outstanding modulation and demodulation concept completely integrated for all kinds of passive contactless communication methods and protocols at 13.56 MHz. The CL RC632 is pin- compatible to the MF RC500, the MF RC530, the MF RC531 and the SL RC400.

The Philips IC CL RC632 supports all layers of the ISO/IEC 14443A/B communication scheme, given correct implementation of additional components, like oscillator, power supply, coil etc. and provided that standardised protocols, e.g. like ISO/IEC 14443-4 and/or ISO/IEC 14443 type B anticollision are correctly implemented. The use of this Philips IC according to ISO14443 Type B might infringe third party patent rights.

A purchaser of this Philips IC has to take care for appropriate third party patent licenses.

The CL RC632 supports contactless communication using MIFARE® Higher Baudrates. The receiver part provides a robust and efficient implementation of a demodulation and decoding circuitry for signals from ISO/IEC 14443 compatible transponders.
The digital part handles the complete ISO/IEC 14443 framing and error detection (Parity & CRC). Additionally it supports the fast MIFARE® Classic security algorithm to authenticate MIFARE® Classic (e.g. MIFARE® Standard, MIFARE® Light) products.

The CL RC632 supports all layers of I•CODE1 and ISO/IEC 15693.
The receiver part provides a robust and efficient implementation of a demodulation and decoding circuitry for signals from I•CODE1 and ISO/IEC 15693 compatible transponders.
The digital part handles I•CODE1 and ISO/IEC 15693 framing and error detection (CRC).

The internal transmitter part is able to drive an antenna designed for proximity operating distance (up to 100 mm) directly without additional active circuitry.

A comfortable parallel interface, which can be directly connected to any 8-bit µ-Processor gives high flexibility for the reader/terminal design.

Additionally a SPI compatible interface is supported

1.2 Features

- Highly integrated analog circuitry to demodulate and decode card response
- Buffered output drivers to connect an antenna with minimum number of external components
- Proximity operating distance (up to 100 mm)
- Supports ISO/IEC 14443 A & B
- Supports MIFARE® Dual Interface Card ICs and supports MIFARE® Classic protocol
- Supports contactless communication with higher baudrates up to 424kHz
- Crypto1 and secure non-volatile internal key memory
- Supports I•CODE1 and ISO/IEC 15693
- Pin-compatible to the MF RC500, MF RC530, MF RC531and the SL RC400
- Parallel µ-Processor interface with internal address latch and IRQ line
- SPI compatible interface
- Flexible interrupt handling
- Automatic detection of the used µ-Processor interface type
- Comfortable 64 byte send and receive FIFO-buffer
- Hard reset with low power function
- Power down mode per software
- Programmable timer
- Unique serial number
- Bit- and byte-oriented framing
- Internal oscillator buffer to connect 13.56 MHz quartz, optimised for low phase jitter
- 3.3 V to 5 V operation for transmitter (antenna driver) in short range and proximity applications
- 3.3 V or 5V operation for the digital part

1.3 Applications

The CL RC632 is tailored to fit the requirements of various applications using contactless communication based on the established ISO/IEC standards operating on 13.56 MHz, as the ISO/IEC 14443 and ISO/IEC 15693 where cost-effectiveness, small size, high performance with a single voltage supply are important.

- Public transport terminals
- Handheld terminals
- On board units
- Contactless PC terminals
- Metering
- Contactless public phones
- supply chain management

2 BLOCK DIAGRAM

The block diagram shows the main internal parts of the CL RC632.

The parallel µController interface automatically detects the kind of 8 bit parallel interface connected to it. It includes a comfortable bi-directional FIFO buffer and a configurable interrupt output. This gives the flexibility to connect a variety of µC, even low cost devices, still meeting the requirements of high speed contactless transactions.

Additionally a serial peripheral interface (SPI) compatible interface will be supported. The CL RC632 acts as a slave during the SPI communication. The SPI clock SCK has to be generated by the master. The SPI interface includes a comfortable bi-directional FIFO buffer.

The Data processing part performs parallel serial conversion of the data. It supports framing including CRC and parity generation / checking. It operates in full transparent mode thus supporting all layers of ISO/IEC 14443 A& B and ISO/IEC 15693.

The status and control part allows configuration of the device to adapt to environmental influences and to adjust to operate with best performance.

For communication with MIFARE® Classic products like MIFARE® Standard or MIFARE® Light a high speed CRYPTO 1 stream cipher unit and a secure non-volatile key memory is implemented.

The analog circuit includes a transmitting part with a very low impedance bridge driver output. This allows an operating distance up to 100mm. The receiver is able to detect and decode even very weak responses. Due to a highly sophisticated implementation the receiver is no longer a limiting factor for the operating distance.

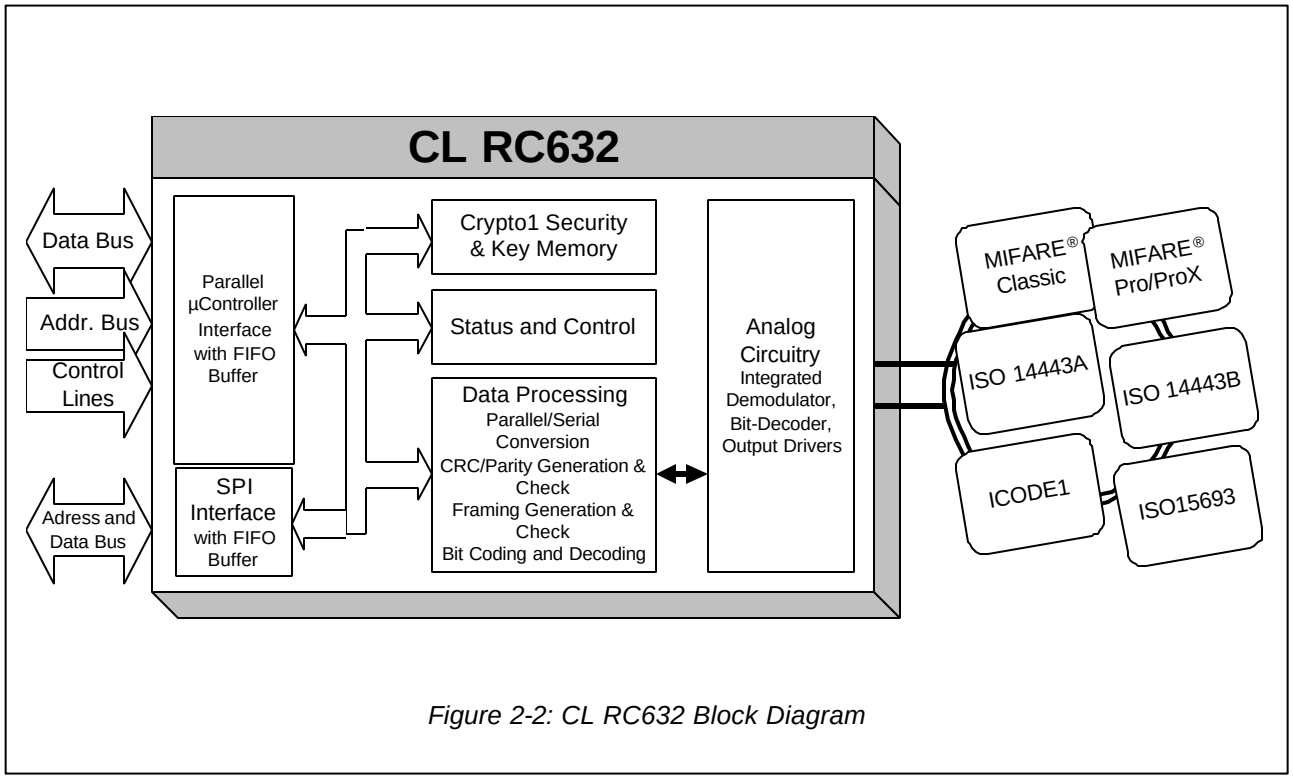

Figure 2-2: CL RC632 Block Diagram

3 CL RC632 PINNING

3.1 Pinning Diagram

The device is packaged in a 32 pin SO-package.

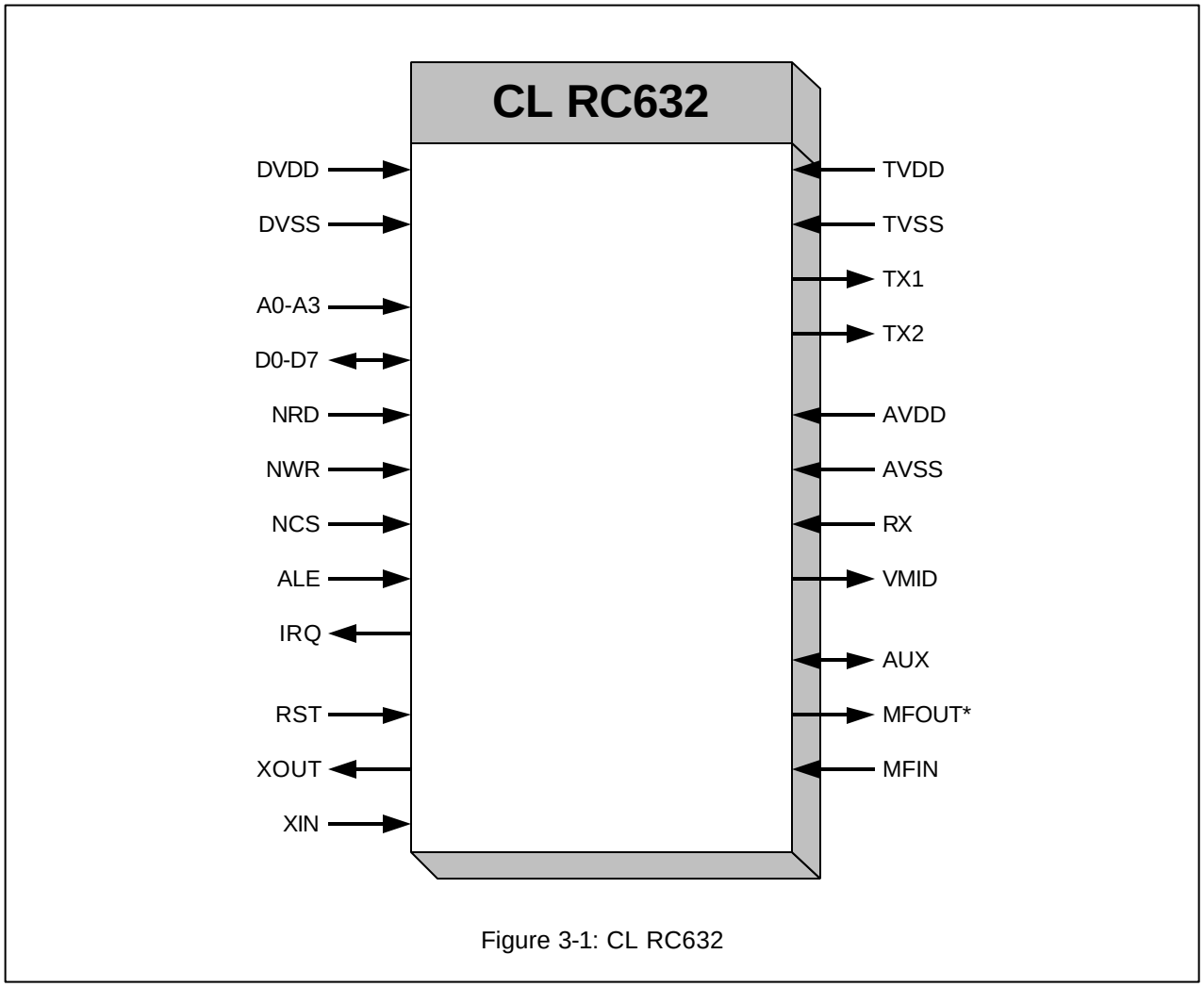

Figure 3-1: CL RC632

The device operates with 3 individual power supplies for best performance in terms of EMC behaviour and signal de-coupling. This gives outstanding RF performance and also maximum flexibility to adapt to different operating voltages of digital and analog part.

*Note: The SL RC400 uses the name SIGOUT for the MFOUT pin. The CLRC 632 functionality includes the test possibilities for the SL RC 400 using the pin MFOUT.

3.2 Pin Description

3.2.1 ANTENNA INTERFACE

The contactless antenna interface basically uses four pins:

Name	Type	Function
TX1, TX2	O Buffered	Antenna Drivers
VMID	Analog	Reference Voltage
RX	I Analog	Antenna Input Signal

To drive the antenna the CL RC632 provides the energy carrier of 13.56 MHz through TX1 and TX2. This signal is modulated by the transmitting data according the register settings.

The card responds with load modulation of the RF field. The resulting signal picked up by the antenna is coupled out from the antenna matching circuit and forwarded to the RX-pin. Inside the CL RC632 the receiver senses and demodulates the signal and processes it according to the register settings. Data is passed further on to the parallel interface where it is accessible by the µ-Controller.

The CL RC632 uses a separate power supply for the driver stage.

Name	Type	Function
TVDD	Power	Transmitter Supply Voltage
TVSS	Power	Transmitter Supply Ground

3.2.2 ANALOG SUPPLY

For best performance the CL RC632 analog part has a separate supply. It powers the oscillator, the analog demodulator and decoder circuitry.

Name	Type	Function
AVDD	Power	Analog Positive Supply Voltage
AVSS	Power	Analog Supply Ground

3.2.3 DIGITAL SUPPLY

The CL RC632 uses a separate digital supply.

Name	Type	Function
DVDD	Power	Digital Positive Supply Voltage
DVSS	Power	Digital Supply Ground

3.2.4 AUXILLARY PIN

Internal signals may be selected to drive this pin. It is used for design-in support and test purpose.

3.2.5 RESET PIN

The reset pin disables internal current sources and clocks and detaches the CL RC632 virtually from the µC bus. If RST is released, the CL RC632 executes the power up sequence.

3.2.6 OSCILLATOR

Name	Type	Function
XIN	I	Oscillator Buffer Input
XOUT	O	Oscillator Buffer Output

The very fast on-chip oscillator buffer operates with a 13.56 MHz crystal connected to XIN and XOUT. If the device shall operate with an external clock it may be applied to pin XIN.

3.2.7 MIFARE® INTERFACE

The CL RC632 supports the active antenna concept of MIFARE®. It may handle the base-band signals NPAUSE and KOMP of MIFARE® Core Modules (MF CMxxx) at the pins MFIN and MFOUT.

Name	Type	Function
MFIN	I with Schmitt Trigger	MIFARE® Interface Input
MFOUT	O	MIFARE® Interface Output Signal Output

The MIFARE® interface may be used to communicate with either the analog or the digital part of the CL RC632 separately in the following ways:

- The analog circuit may be used stand-alone via the MIFARE® interface. In that case MFIN will be connected to the externally generated NPAUSE signal. The MFOUT pin provides the KOMP signal.
- The digital circuit may be used to drive an external analog circuit via the MIFARE® interface. In that case the MFOUT pin provides the internally generated NPAUSE signal and MFIN will be connected to the KOMP signal from the outside.

Note: The SL RC400 uses the name SIGOUT for the MFOUT pin. The CLRC 632 functionality includes the test possibilities for the SL RC 400 using the pin MFOUT.

3.2.8 PARALLEL INTERFACE

16 pins control the parallel interface:

Name	Type	Function
D0 … D7	I/O with Schmitt Trigger	Bi-directional Data Bus
A0 … A2	I/O with Schmitt Trigger	Address Lines
NWR / RNW	I/O with Schmitt Trigger	Not Write / Read Not Write
NRD / NDS	I/O with Schmitt Trigger	Not Read / Not Data Strobe
NCS	I/O with Schmitt Trigger	Not Chip Select
ALE	I/O with Schmitt Trigger	Address Latch Enable

IRQ	O	Interrupt Request

3.2.9 SPI COMPATIBLE INTERFACE

4 pins control the SPI compatible interface.

Name	Type	Function
A0	I/O with Schmitt Trigger	MOSI, master to slave communication
A2	I/O with Schmitt Trigger	SCK, clock to be generated by the master
D0	I/O with Schmitt Trigger	MISO, slave to master communication
ALE	I/O with Schmitt Trigger	NSS, enables the SPI communication

3.3 Applications

3.3.1 CONNECTING DIFFERENT µCONTROLLER'S

The CL RC632 supports different parallel µC interfaces and a SPI compatible interface. An intelligent auto-detection logic automatically adapts the parallel interface to the respective bus system. Selection of the device is performed with signal NCS.

To connect µ-Controllers using separated address and data bus pin ALE has to be connected to DVDD.

To connect µ-Controllers using multiplexed address and data bus pin ALE has to be connected to the signal ALE of the µ-Controller

To connect µ-Controllers using RNW and NDS (instead of NWR and NRD) the µ-Controller’s RNW has to be connected to pin NWR and NDS to pin NRD.

3.3.2 APPLICATION EXAMPLE

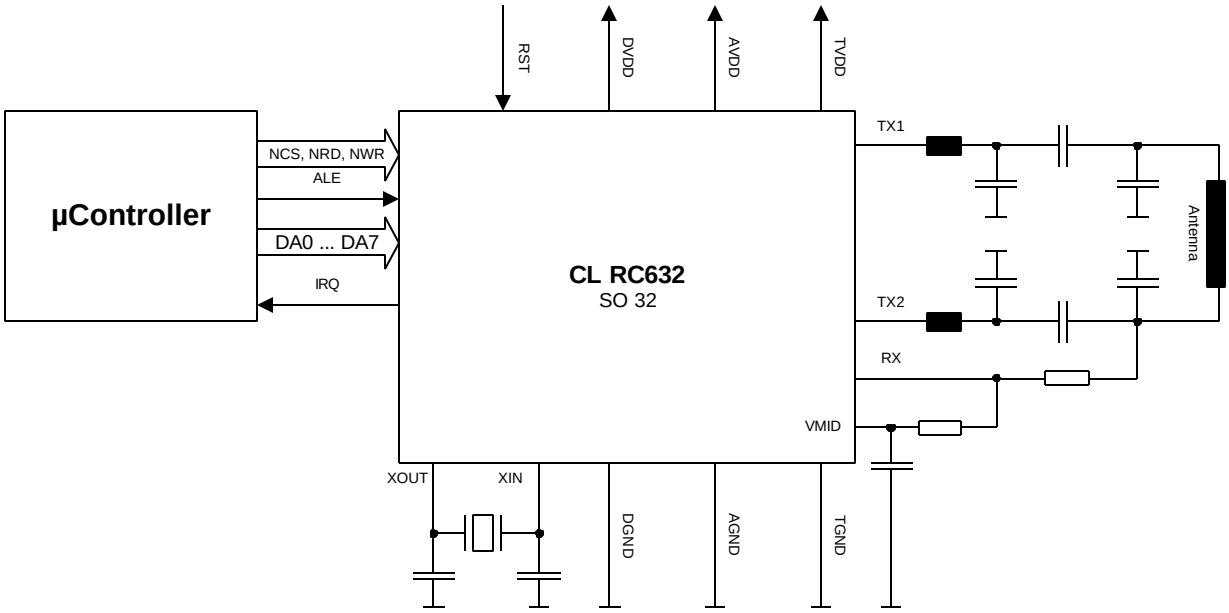

Figure 3-2: CL RC632; Principle circuit for short distance

4 MIFARE® CLASSIC RELATED ITEMS

4.1 CRYPTO I: Card Authentication

For correct authentication of MIFARE® Classic products the fast CRYPTO 1 stream cipher is available. The corresponding keys have to be programmed into the secure non-volatile key memory of the CL RC632.

Only two commands need to be sent by application software to turn on CRYPTO 1 secured communication.

4.1.1 INITIATING CARD AUTHENTICATION

The correct key for the authentication has to be selected from the secure internal non-volatile key memory and loaded into the internal CRYPTO1 register. Next the authentication command is transmitted to the card.

After receiving the first message token from the card, the µ-Controller has to check the communication status flags. If communication so far has been successful the second part of the authentication procedure can be started.

4.1.2 SECOND PART OF CARD AUTHENTICATION

Data to be transmitted to the card in this phase are generated automatically by the internal CRYPTO 1 unit inside the CL RC632. To request this action the according command has to be triggered.

The card will respond with the second message token. Then the communication status flags have to be checked by the µ-Controller. If authentication has been successful further communication with a MIFARE® Classic card continues CRYPTO 1 enciphered.

5 ELECTRICAL SPECIFICATION

5.1 DC Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Voltage Supply						
DVDD	Digital Supply Voltage		4.5	5.0	5.5	V
			3.0	3.3	3.6	
AVDD	Analog Supply Voltage		4.5	5.0	5.5	V
TVDD	Transmitter Supply Voltage		3.0	5.0	5.5	V
Current Consumption						
I_{DVDD}	Operating Digital Supply Current	Idle Command		6	9	mA
I_{AVDD}	Operating Analog Supply Current	Idle Command, Receiver On		25	40	mA
I_{TVDD}	Operating Buffered Antenna Driver Supply Current	continuous wave			150	mA

5.2 Start up Characteristics

Mode	CONDITIONS	Current	UNIT	Time	UNIT
Startup times and current consumption					
Power on		-	-	< 500	µs
Hard Reset via Reset Pin		< 1	µA	< 500	µs
Soft Reset via Register Setting		< 1	µA	< 500	µs

6 REVISION HISTORY

REVISION	DATE	CPCN	PAGE	DESCRIPTION
3.2	April 2005		3 13	Update chapter 1.1 with 14443B patent infringement warning Insert Revision History
2.0	June 2002	-		published version
1.0	January 2002	-		internal version

Table 0-1: Document Revision History

Definitions

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics section of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

7 DISCLAIMERS

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